REMARKS

Claims 1-15 are currently active.

The Examiner has rejected Claims 1 and 9 as being anticipated by Gorshe. Applicant respectfully traverses this rejection in view of the amendments to the claims. Claims 1 and 9 now recite the second rate is different from the first rate; and pursuant to the Examiner's comments on page 4, paragraph 2, it is respectfully submitted Claims 1 and 9 are now allowable.

Referring to Gorshe, there is taught an interfacing device 5 performs the basic functions essential to carrying out the objectives of the invention taught by Gorshe. The interface device has a pair of input ports 10, 12, a pair of output ports 14, 16, and a pair of bi-directional ports 18, 20. The timing and synchronization aspects of the interface device are handled through the primary clock input 22, the primary frame pulse input 24, the reference clock output 26, and the reference frame pulse output 28. When the interface device is implemented in a receive path, data from a tributary units flow into one or both of the input ports 10, 12. The data may also flow into the interface device through one or both of the bi-directional ports 18, 20 and from neighboring interface devices with which it is cascaded. All data latched into the device by the input port data latches 30, 32 is made available to the time slot assignment portions of the device. The swap offers 38, 40 perform time slot assignment

functions on the data which is presented to them by the latch is 34, 36. See column 6, lines 40-65.

When the device is implemented in a transmit path, data from the TSI units flow into one of both of the input ports 10, 12. All data latched into the device by the input port data latches 30, 32 is made available to the time slot assignment portions of the path. As with the receive path operation, the 4:1 selection data latches 34 and 36 functions to route any of the nine-bit wide input data rails to the swap buffers 38, 40, which perform time slot assignment functions on the data which is presented to them by the latches 34, 36. See column 7, lines 5-16. As is clear from the above description of the operation of the architecture taught by Gorshe, data rails are used to transfer the input data from the input port to an output port at the same rate.

Accordingly, Claims 1 and 9, as amended, are now patentable over Gorshe.

The Examiner has objected to Claims 2-8 and 10-15.

In view of the foregoing remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-15, now in this application be allowed.

Respectfully submitted,

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